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EXAMINER

NGUYEN, KHIEM D

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 8-11 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Sahin et al. (U.S. Patent 2003/0220708).

In re claim 8, Sahin discloses a system for creation of an opening of controllable format through a layer of insulation material, comprising:

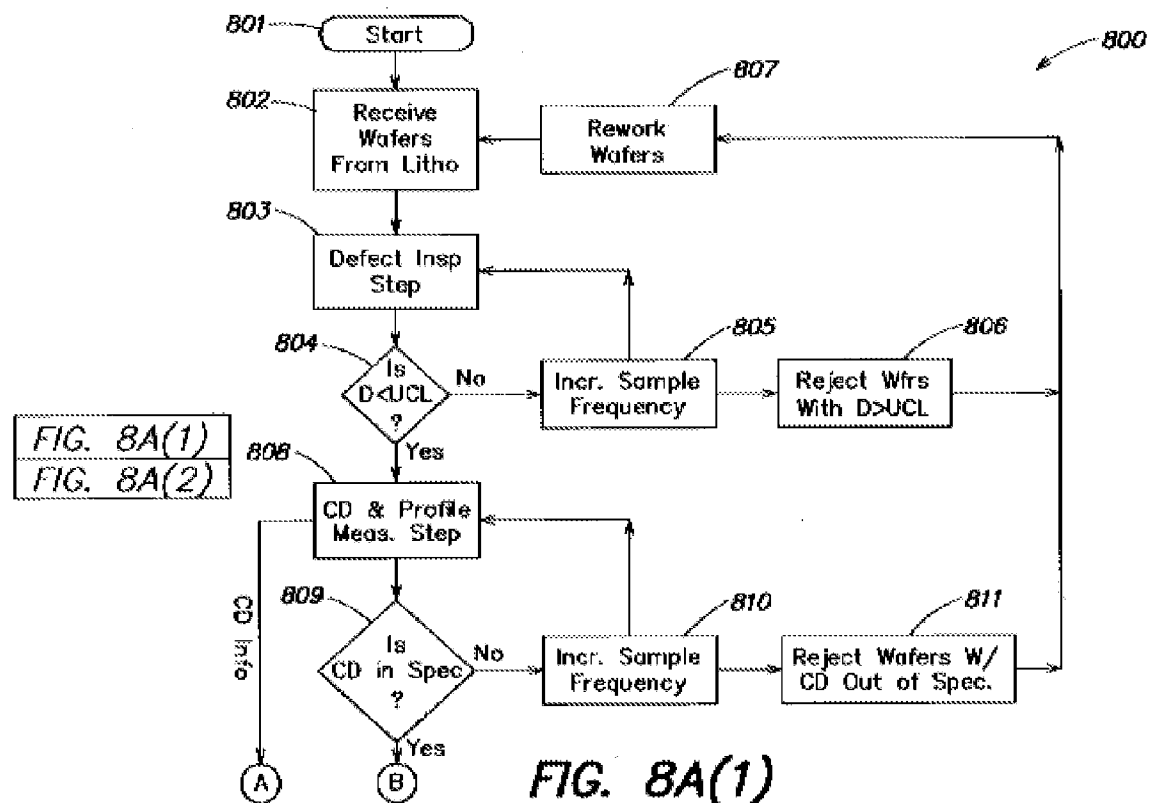
means **102** for creating an opening **710a**, **710b** through a layer of etch resist material **708** provided over the surface of a layer of insulating material **704/706** having been deposited over the surface of a substrate **702** (see page 11, paragraphs [0150]-[0152] and FIGS. 7A-C);

means for measuring an obtained critical dimension measurement of the opening **710a**, **710b** created through the layer of etch resist material **708** (see page 16, paragraph [0207] and step 803 in FIG. 8A(1));

means, including a feedback mechanism (see page 12, paragraph [0166]), for assuring that the obtained critical dimension measurement of the opening created through the layer of etch resist material **708** is within design specification

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(see page 16, paragraph [0210] and step **809** in FIG. 8A(1)), the feedback mechanism communicating with the means for creating an opening through a layer or etch resist material **708** to control the critical dimension (CD) measurement of the opening **710a**, **710b** by implementing corrections (see step **807**) in the means for creating an opening through a layer of etch resist material (see page 6, paragraph [0211] and steps **807** and **810** of FIG. 8A(1));



means for creating an opening **710a**, **710b** through the layer of insulation material **704/706**, whereby a diameter of the opening **710a**, **710b** through the layer of insulation material **704/706** is dependent on a diameter of the opening

**710a, 710b** created through the layer of etch resist material **708** (see page 17, paragraphs [0214]-0215); and

means, including a feedback mechanism, for assuring that the opening **710a, 710b** created through the layer of insulation material **704/706** is within design specification (see page 17, paragraphs [0216]-[0219]).

In re claim 9, as applied to claim 8 above, **Sahin** discloses all claimed limitations including the limitation wherein means, including a feedback mechanism (see page 12, paragraph [0166]), for assuring that an obtained critical dimension measurement of the opening **710a, 710b** created through the layer of etch resist material **708** is within design specification comprising (see page 16, paragraph [0210] and step **809** in FIG. 8A(1)): means for linking to a software supervisory function, thereby including data transmission functions, means for linking to a software function equally being linked to a software supervisory function, thereby including data transmission functions; means for data manipulating capabilities, thereby including manipulating interdependent data ; means for interfacing with semiconductor equipment, thereby including equipment functioning in a supporting role to the semiconductor equipment; and means for creating instructions for the semiconductor equipment, thereby including equipment functioning in a supporting role to the semiconductor equipment (see page 6, paragraph [0094]).

In re claim 10, as applied to claim 8 above, **Sahin** discloses all claimed limitations including the limitation wherein means for assuring that the opening

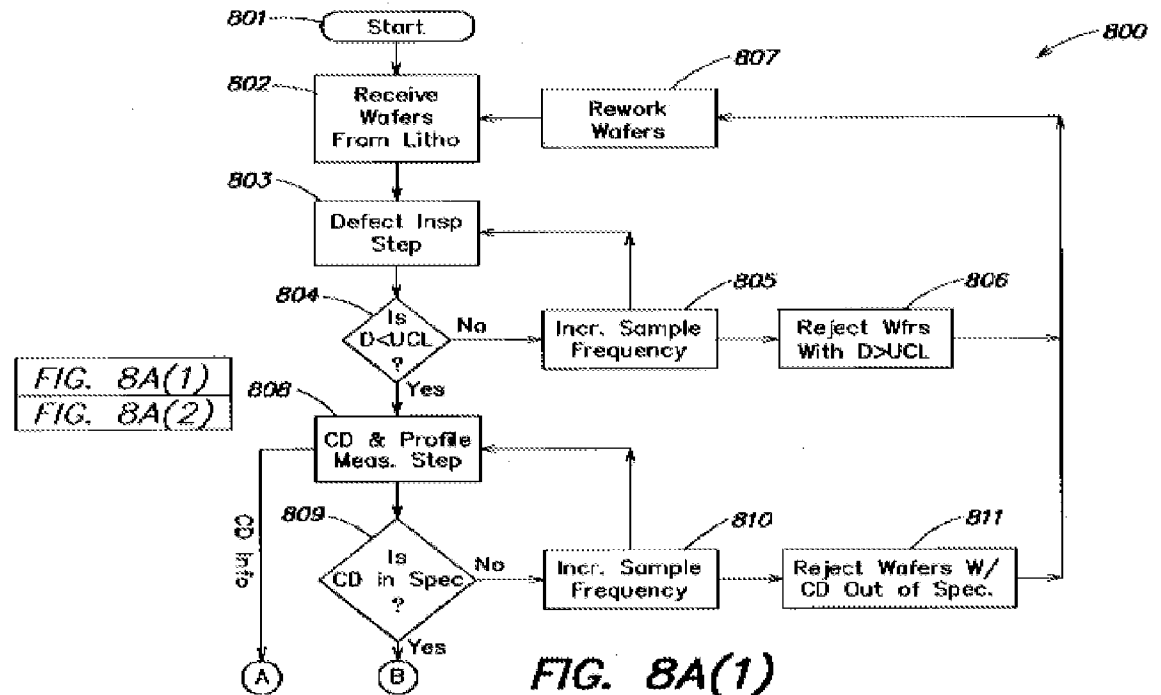
**710a 710b** created through the layer of insulation material **704/706** is within design specification comprising: means for linking to a software supervisory function , thereby including data transmission functions, means for linking to a software function equally being linked to a software supervisory function, thereby including data transmission functions; means for data manipulating capabilities, thereby including manipulating interdependent data; means for interfacing with semiconductor equipment, thereby including equipment functioning in a supporting role to the semiconductor equipment; and means for creating instructions for the semiconductor equipment, thereby including equipment functioning in a supporting role to the semiconductor equipment (see page 6, paragraph [0094]).

In re claim 11, as applied to claim 8 above, **Sahin** discloses all claimed limitations including the limitation wherein the system further comprising means for creating an opening **710a, 710b** having non-linear sidewalls through a layer of insulation material by applying a high-polymer based etch to the surface of the layer of insulation material **704/706** (see page 11, paragraph [0158]).

In re claim 15, **Sahin** discloses a system for creation of an opening of controllable format through a layer of insulation material, comprising:

means **102** for creating an opening **710a, 710b** through a layer of etch resist material **708** provided over the surface of a layer of insulating material **704/706** having been deposited over the surface of a substrate **702** ((page 11, paragraphs [0150]-[0152] and FIGS. 7A-C);

means, including a feedback mechanism (see page 12, paragraph [0166]), for obtaining a critical dimension measurement of the opening created through the layer of etch resist material **708** assuring that the critical dimension measurement (CD) is within design specification (see page 16, paragraph [0210] and step **809** in FIG. 8A(1)), the feedback mechanism communicating with the means for creating an opening **710a**, **710b** through a layer of etch resist material **708** to control the critical dimension measurement (CD) of the opening **710a,710b** (see page 6, paragraph [0211] and steps 807 and 810 of FIG. 8A(1));



means for creating an opening **710a**, **710b** having non-linear sidewalls through the layer of insulation material **704/076** by applying a high-polymer based etch to the surface of the layer of insulation material **704/706** (see

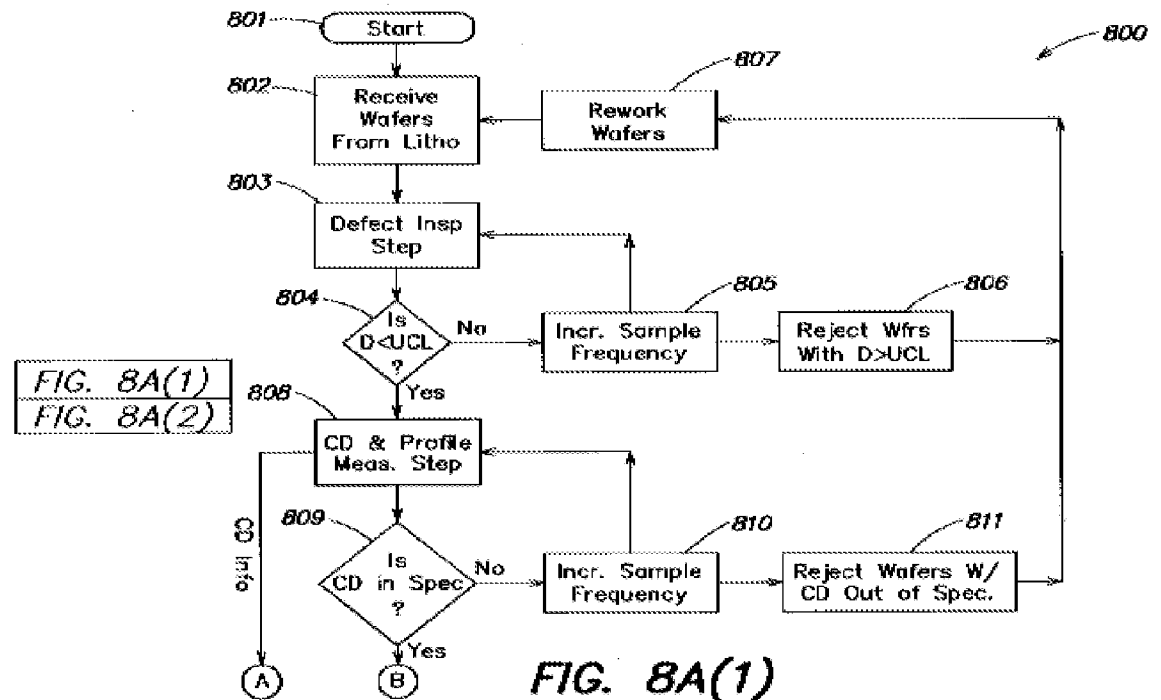
paragraph [0158]), whereby a diameter of opening having non-linear sidewalls is dependent on a diameter of the opening created through the layer of etch resist material **708** (see page 17, paragraphs [0214]-[0215]); and

means, including a feedback mechanism, for assuring that the opening **710a, 710b** created through the layer of insulation material **704/706** is within design specification (see page 17, paragraphs [0216]-[0219]).

In re claim 16, Sahin discloses a system for creation of an opening of controllable format through a layer of insulation material, comprising:

means, including a feedback mechanism (see page 12, paragraph [0166]), for creating an opening **710a, 710b** through a layer of etch resist material **708** provided over the surface of a layer of insulating material **704/706** having been deposited over the surface of a substrate **702**, such that the opening **710a, 710b** has a critical dimension measurement (CD) that is within design specification (see page 16, paragraph [0210] and step 809 in FIG. 8A(1));





means for creating an opening **710a**, **710b** through the layer of insulation material **704/706**, whereby a diameter of layer of insulation material **704/706** is dependent on a diameter of the opening **710a**, **710b** created through the layer of etch resist material **708** (see page 17, paragraphs [0214]-[0215]); and

means, including a feedback mechanism, for assuring that the opening created through the layer of insulation material is within design specification (see page 17, paragraphs [0216]-[0219]).

In re claim 17, as applied to claim 16 above, **Sahin** discloses all claimed limitations including the limitation wherein the means, including a feedback mechanism, for creating an opening **710a**, **710b** (see page 12, paragraph [0166]) include means for making corrections to an original critical dimension

measurement (CD) that is not within design specification (see page 17, paragraphs [0214]-[0215]).

***Allowable Subject Matter***

3. Claims 12-14 were previously allowed over prior art of record as indicated in the Office Action, Paper No. 030305 mailed on March 08<sup>th</sup>, 2005.

***Response to Applicants' Amendment and Arguments***

4. Applicants' arguments filed on April 1<sup>st</sup>, 2008 have been fully considered but they are not persuasive.

Applicants contend that the reference, Sahin et al. (U.S. Pub. 2003/0220708), herein known as **Sahin** provides no feedback mechanism that communicates with the means for creating an opening through a layer of etch resist material to control the CD (critical dimension) of the opening.

In response to Applicants' contention that **Sahin** does not teach or suggest that the feedback mechanism communicating with the means for creating an opening through a layer of etch resist material to control the critical dimension (CD) measurement of the opening,

Applicants' attention is respectfully directed to (page 6, paragraphs [0209]-[0211] and FIGS. 8A(1), for example), where **Sahin** discloses step **808** of measuring the critical dimension (CD) and profile of the processed wafer, step **809** of checking to assure if the CD is within the design specification, if the processed wafer having CD that out of the design specification, reject the wafer

(see step **811**) and send the wafer back for rework through photolithographic tool (see steps **807** and **802**).

Thus, in view of the above, **Sahin** clearly discloses a feedback mechanism that communicating with the photolithographic tool and the checking and measuring tool in order to assure that the CD obtained is within the design specification and to control the CD measurement of the opening by implementing corrections in the means for creating an opening through a layer of etch resist material.

For this reason, Examiner holds the rejection proper.

### ***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time Policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### ***Correspondence***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/  
Examiner, Art Unit 2823  
/W. David Coleman/  
Primary Examiner, Art Unit 2823